AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 0014 with the following amended paragraph:

Turning now to the drawings, and, more particularly, Figure 1 shows a cross section of a preferred embodiment durable array pad 100 on a semiconductor chip or wafer 102 at a terminal metallurgy pad 104, e.g., aluminum (Al), connected through a terminal via to the underlying chip wiring 105 ~~(not shown)~~. The terminal via extends through typical wafer/chip passivation layers, e.g., a nitride layer 106 overlying an oxide layer 108. A final passivation layer, e.g., polyimide layer 110, formed on the terminal metallurgy pad layer has vias to each of the terminal metallurgy pads 104. A diffusion barrier pad 112 is formed on the terminal metallurgy pads 104. The preferred diffusion barrier pad 112 is a layered pad of tantalum/tantalum nitride (Ta/TaN) or titanium/titanium nitride (Ti/TiN) or a layer pad of materials selected from titanium tungsten (TiW), chromium (Cr) with an adhesion layer of chrome-copper (CrCu), titanium (Ti) or nickel vanadium (NiV) formed on the barrier metallurgy. A copper (Cu) seed layer 114 is formed on the barrier metal pads 112, which provides a conducting seed layer for electroplating. Hard test barrier pads 116 are formed on the copper seed layer pads 114, preferably, by plating the copper seed layer pads 114 with nickel (Ni). Finally, the hard barrier pads 116 are passivated with a passivating barrier layer 118, e.g., gold (Au), ruthenium (Ru), rhodium (Rh) or copper. Solder balls (C4s) may be formed on the completed pads 100, even after the chip is tested by application of test probes directly to the pads 100. Thus, subsequent bump, bond and assembly options are expanded, allowing for selecting a suitable final connect for particular application (or manufacturing capacity) needs. Further, because C4s are formed after test, they not deformed during test, allowing finer C4 pitch, e.g., 3 mil bump pitches and finer.

Please replace paragraph 0016 with the following amended paragraph:

Figures 3A – H show in a cross section, formation of preferred embodiment pads on the surface of a wafer according to the present invention. So, first in step 122 as shown in the cross section 140 of Figure 3A, after forming circuit layers on a wafer 142 and terminal metallurgy pads (104 in Figure 1), e.g., after normal back end of the line (BEOL) processing. The[[,]] seed metal layers 144, 146 are formed on the final passivation layer (e.g., 110 in Figure 1) on the wafer 142. A 500 – 20,000 angstrom (20,000ℓ) conductive barrier layer 144, which corresponds to pad layer 112 in Figure 1, is formed on the upper surface 148 of the wafer 142. Preferably, conductive barrier layer 144 is a 2500ℓ thick layer of a suitable barrier material (TiW, Cr, Ta/TaN, Ti/TiN) or adhesion material (CrCu, Ti or NiV) or a combination thereof. Then, a 500 – 50,000ℓ thick seed material layer 146 terminating in copper is formed on the barrier/adhesion layer 144. Preferably, the seed material layer 146 is a one micrometer (1μm or 10,000ℓ) thick copper layer. Seed pads are defined in step 124 by first forming a block out mask 150 on the seed layer 146 as shown in Figure 3B. Preferably, the block out mask 150 is formed using any suitable technique, e.g., forming a photo resist layer and patterning the resist photolithographically. Then, with the developed resist mask 150 on the seed layer 146 reflecting the pad pattern, the exposed portions of the seed layer 146 are removed, e.g., etched to leave copper pads 152 (corresponding to pad layer 114 in Figure 1) on the barrier/adhesion layer 144 as shown in Figure 3C.

Please replace paragraph 0017 with the following amended paragraph:

Plating the seed pads 152 in step 126 begins by removing the mask pattern to expose the seed pads 152 as shown in Figure 3D. Then, a hard test barrier layer 154 is formed on the seed pads 152 in Figure 3E, e.g., plating the seed pads 152 with a 0.5 – 30μm and preferably, a 1μm thick layer of nickel. In Figure 3F, the hard test barrier layer 154 (corresponding to pad layer 116 in Figure 1) is passivated with application of a

suitable nickel barrier metal 156 (corresponding to 118 in Figure 1) for solder adhesion. Preferably, a 200 – 1,000ℓ thick Au, Ru, Rh or Cu layer 156 passivates the hard test barrier layer 154 and, in particular, a 500ℓ Au, Ru or Rh layer and/or 5,000ℓ of Cu. Optionally, a corrosion inhibitor such as benzotriazole (BTA) may also be included for passivating a copper test barrier layer 154. Any such corrosion inhibitor that may be included, must be readily removable, e.g., with cleaning solvent or with heat below 200°C. Once passivated, the pads 152 are completed in step 124 as shown in Figure 3G by etching the diffusion barrier layer 144, masked/patterned by the pads 152.